

APPLICATION NOTE

200mm <100> NTD SILICON WAFERS FOR HIGH POWER

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Abstract. It is demonstrated that Neutron Transmutation Doped 200 mm wafers have excellent resistivity uniformity and that the resistivity stability after high temperature processing of NTD wafers is very well controlled.

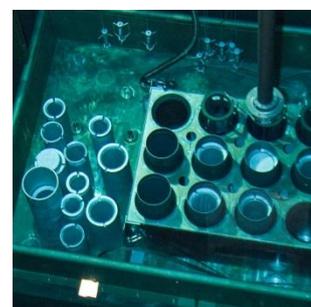
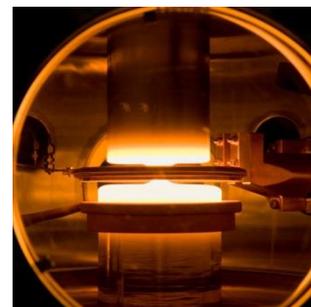
Introduction

Topsil has a well-established history in supplying neutron transmutation doped (NTD) float zone (FZ) silicon wafers for the very high and high power electronic market. The NTD product has been carefully designed in order to meet the market requirements of extremely high resistivity uniformity and stability upon subsequent wafer processing. Our standard capability covers the resistivity range 20-1500 Ω -cm for 2-5 inch and the resistivity range 20-800 Ω -cm for 150 mm and 200 mm <100>.

This product application note covers a 200 mm <100> NTD product in the resistivity range 20-800 Ω -cm with equally high capability in terms of resistivity uniformity and stability. This product, however, has some distinct features which require clarification in order for the customer to appreciate the product properties. The scope of this application note is to describe the capability and material properties of this product.

Product properties

The product has tight resistivity control with deviations from specification of target resistivity less than 7%, radial resistivity variation (RRV) less than 7%, and striations less than 10%. The product resistivity also shows excellent thermal stability after processing. The point defect properties are carefully designed, and contamination is carefully controlled to give a high GOI yield, above 90% and wafer lifetimes above 300 μ s.



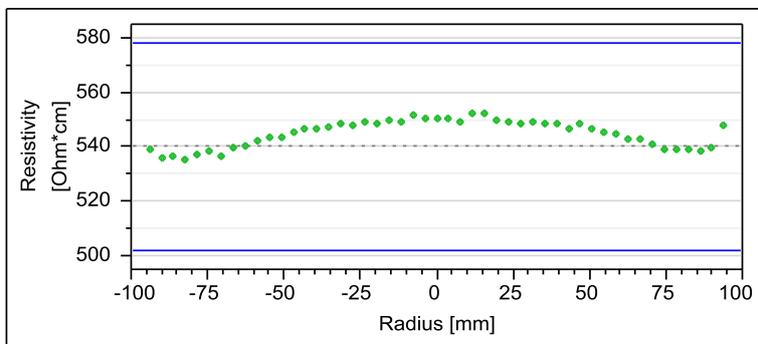
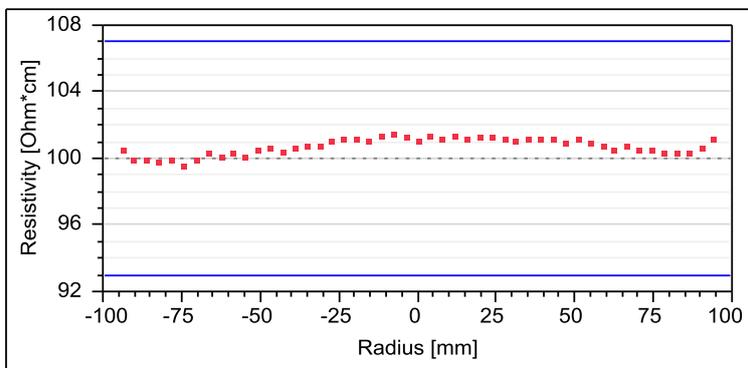


Figure 1. Typical wafer radial resistivity profile after 4 hour 1100°C annealing treatments. The blue lines indicate a tolerance of $\pm 7\%$.

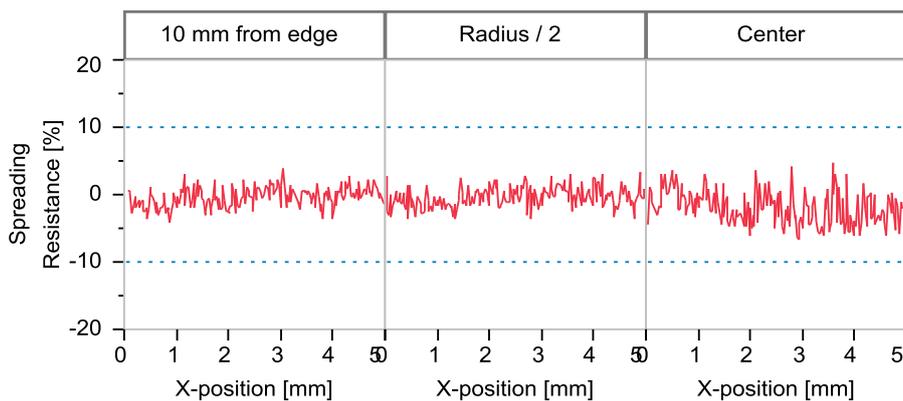


Figure 2. Striations are not detectable after wafer heat treatment. The dotted blue lines indicate typical specification limits of $\pm 10\%$.

Product Design

Topsil has designed the process in such a way that the uniform and stable resistivity reached after high temperature thermal treatment is centred at the target resistivity specified by the customer. This procedure ensures that the resistivity after wafer processing, which is the value relevant to the customer, is within specification.

The ingot has not been annealed after irradiation, and therefore the lattice damage from irradiation is not recovered on the as delivered wafers. The lattice will recover after the first high temperature processing step during device processing. It is not possible to measure neither resistivity nor lifetime on the as-received wafers until after the first high temperature processing step. After the first annealing step above 1050°C all points on the wafer are well within customer specification.

The accept criterion for shipping wafers to customers is that the resistivity from two sample wafers, one from each end of the ingot, is within specification after an annealing step at 1100°C. The wafers are measured according to a modified SEMI MF81 plan C. The resistivity from these two wafers will be provided in the certificate of analysis supplied with the wafers. The lifetime is guaranteed and the minimum value of 300 μ s will be provided in the certificate of conformance delivered with the wafers.

In order to verify the behaviour of resistivity and lifetime after thermal processing, Topsil will provide running control charts of average resistivity, RRV, and lifetime by carrying out high temperature heat treatment of test wafers from each batch. Examples of such control charts are shown in the figures 3, 4 and 5.

The product resistivity capability after thermal processing is displayed in the table below:

Resistivity range	Tolerance	RRV	Striations
20-800 Ω -cm	$\pm 7\%$	<6%	Not detectable

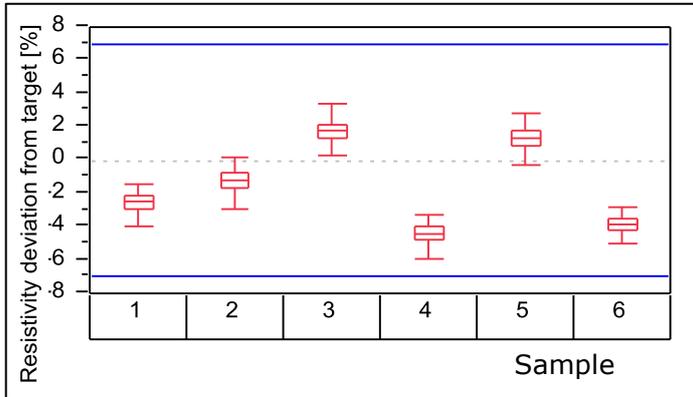


Figure 3. Control chart for average resistivity relative to the resistivity target after wafer heat treatment.

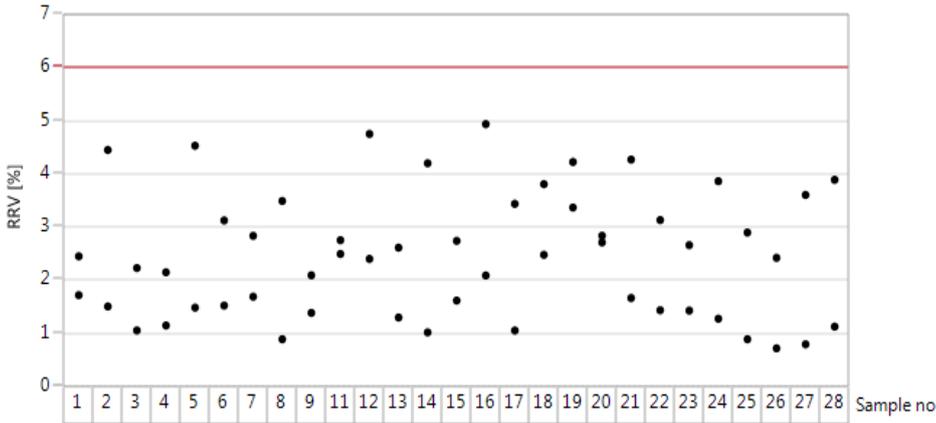


Figure 4. Control chart for radial resistivity variation after wafer heat treatment.

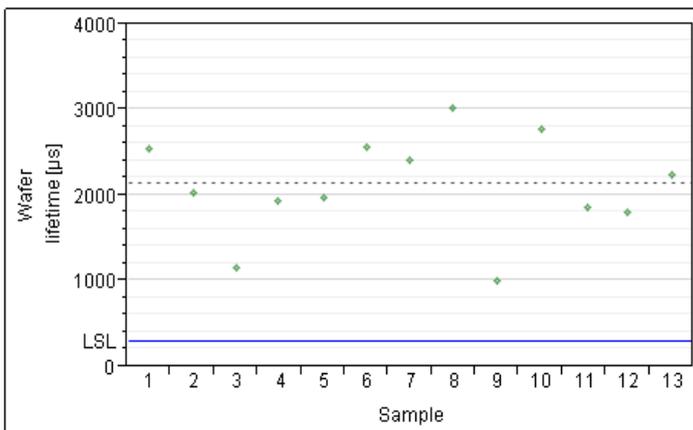


Figure 5. Control chart for lifetime after wafer heat treatment

The resistivity stability after repeated annealing has been tested. Resistivity after 1-5 repeated annealings, 4hour at 1100°C in 5% oxygen in nitrogen atmosphere is shown in figures 6 and 7. A 1-2% decrease in resistivity is seen when wafers are annealed more than once.

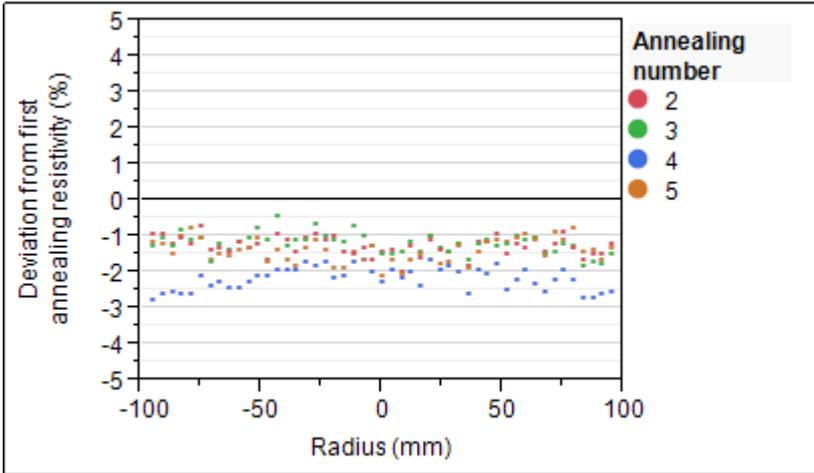


Figure 6. Resistivity stability of a 550 Ohm*cm product during repeated annealings, 4hour at 1100°C in 5% oxygen in nitrogen atmosphere. A 1-2% decrease in resistivity is seen when the wafers are annealed more than once.

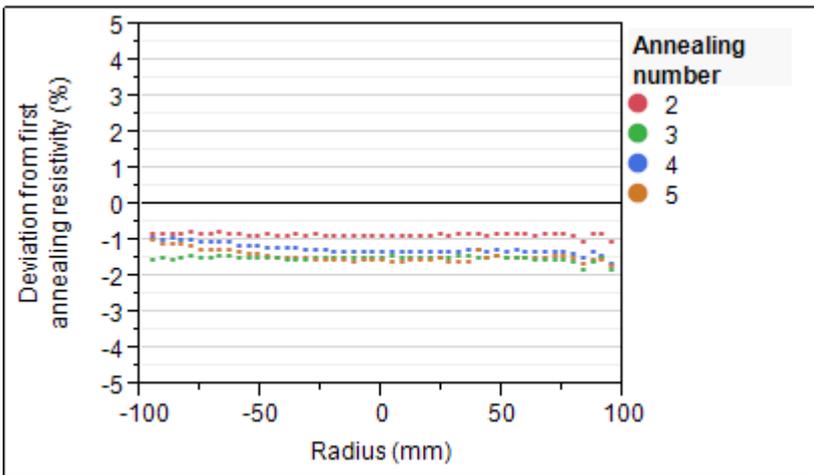


Figure 7. Resistivity stability of a 90 Ohm*cm product during repeated annealings, 4hour at 1100°C in 5% oxygen in nitrogen atmosphere. A 1-2% decrease in resistivity is seen when the wafers are annealed more than once.

Conclusion

This application note covers a 200 mm <100> NTD product in the resistivity range 20-800 Ω -cm with excellent resistivity control and resistivity uniformity after thermal processing.

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Topsil Semiconductor Materials A/S

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