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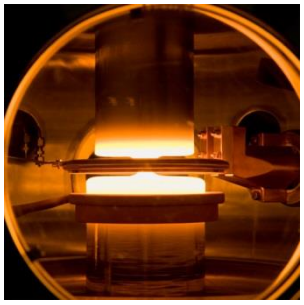
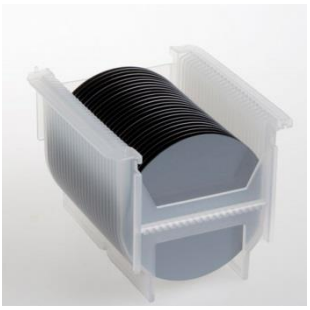
APPLICATION NOTE

PREFERRED FLOAT ZONE (PFZ) SILICON FOR POWER ELECTRONICS

Abstract
This note presents a silicon substrate that - due to its process purity - is well suited for lateral and vertical power devices like Power MOSFET's, IGBT's and high power thyristors. The substrate is manufactured on the basis of gas phase doped Float Zone technology which enables exact resistivity control throughout the whole of the crystal.





Introduction
The quest for perfect monocrystalline silicon has been on for decades. Every time a new matureness level for the silicon material has been reached, the electronics industry puts forward new challenges to the silicon manufacturers. The definition and parameterisation of perfect silicon has been the subject of many research and development projects, primarily within the Czochralski (CZ) growth technique community, where many obstacles in the purification step have hindered an absolute perfect silicon standard to be derived. Most Czochralski products claiming to be perfect silicon have extra processing steps such as hydrogen annealing or intrinsic gettering steps added to the wafering step to assure a pseudo-perfect CZ silicon wafer suitable for electronic device manufacturing.

Float Zone (FZ) technology for growing silicon monocrystalline material is by far the most pure method and results in perfect silicon with unique properties as opposed to any other growth technology. Float Zone silicon can be grown with resistivities exceeding 100.000 Ωcm because of the process purity. Czochralski silicon does not have this high level of purity and it is difficult to grow Czochralski silicon with resistivities exceeding 100 Ωcm. Also, performance degrading impurities such as oxygen is much lower by two orders of magnitude in Float Zone silicon in comparison with Czochralski silicon where crucibles give high and unpredictable levels of oxygen in the bulk of the silicon.

This application note presents the characteristics of in-situ gas phase doped Float Zone silicon, which is hereafter named Preferred Float Zone (PFZ) silicon. PFZ silicon has unique control measures built into the growth process. Dopant distribution is tightly controlled throughout the length of the monocrystalline rod by using stable, manufactural processes. Manufacturing control is essential to be able to maximise production volume and Topsil has put large efforts in controlling such parameters as poly silicon charge weights, total process cycle times and process surveillance. Topsil can meet demand from all parts of the electronics industry on high volume, high quality PFZ n- and p-type material.

Applications of PFZ wafers are multiple. They form the perfect basis for both lateral and vertical power devices like Power MOSFET's, IGBT's and high power thyristors. Indeed, this is the largest market for PFZ wafers and this market is forecasted to grow considerably in the years to come (Yole Developpement, 2014). Driving this growth rate forecast are some megatrends:

- Today, around half of the global energy power device consumption is used for modern conveniences such as computers, offices, consumer, and lighting. Continued urbanisation, and a growing middle class worldwide will call for an increased number of such modern conveniences in the future.

- Due to cost, the vast proportion of the present day motors has no electronic control thereby wasting a lot of energy in comparison with solutions that have inverterised variable speed drives (IGBT's). In recent years, a rapid development of green technologies driven by concern of increased levels of pollution, focus on CO2 emissions, and prices on fossil fuels has taken place. This, in a combination with an overall increased demand for sufficient electricity supply, will make energy saving devices and renewables more attractive in the future.

Summarising the above into one sentence that will be the driver for the power industry for many years ahead could be a phrase something like this:

"Power Management circuitry to improve efficiency in the range from µW to MW"

In addition, the automotive industry is on the move of making "electronic" moving vehicles equipped with lots of power efficient semiconductor circuits to control brakes, steering systems, electrical circuitry and many peripherical electrical systems. Key words for the automotive industry are reliability in harsh environments and small footprint (and thereby weight). Also, silicon based medium and high power devices will play a significant role in the quest for zero emission and hybrid electric automobile motor drives. PFZ wafers are addressing

the needs of the automotive industry by offering high purity wafers with minimum amounts of degrading impurities and semiconductor power devices based on PFZ wafers are thus expected to have superior performance to those based on other silicon semiconductor materials.

The biggest markets for perfect silicon wafers – that is annealed Czochralski wafers with denuded zones free from any BMD's – are the markets for memory chips and digital signal processors DSP's). The annealed wafers offer a lower cost alternative to MOS epitaxial wafers. Some of the concerns regarding production of annealed wafers are temperature homogeneity issues in annealing furnaces and contamination. In case of furnace inhomogeneities and contaminations, the wafers are rendered non-useable for device makers. Furnace temperature inhomogeneities cause stress in the wafers during annealing and will cause large warpage in the finished product.

Contaminants can be difficult to measure in the finished annealed wafer CZ based product, but the contaminants can be activated during device processing and will always have a catastrophic impact on the final device properties.

Perfect PFZ wafers are produced without the need of an extra annealing step and they can be used directly in the manufacturing of memory chips and DSP's, but are also the best starting material for silicon-on-insulator (SOI) products. SOI products are now being introduced into mainstream electronic device processing not only for memory chips and DSP's, but also for microprocessors in general. PFZ wafers are free from contaminants (the contaminant level is always monitored by bulk lifetime control) and the warpage can be controlled by proper handling of the wafer process and will always be lower by ~50% in comparison with annealed wafers.

As indicated above the electronic market is very diverse with many different requirements for basis material characteristics. Topsil is supplying PFZ wafers to the part of the power and the electronics industry requiring perfect silicon. PFZ wafers will continue to emerge into non-electronic applications such as industries requiring good mechanical performance (like the MEMS industry) and industries requiring good optical performance (like the photo detector industry). These industries together with the power and electronics industries are benefiting from using perfect silicon in the form of prime PFZ wafers.

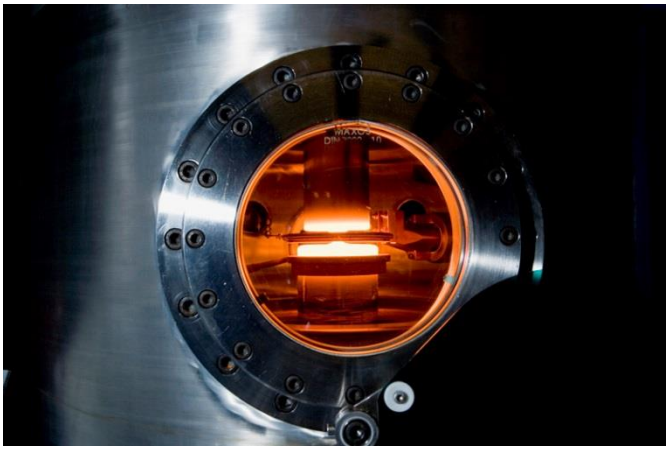


Figure 1. Picture of the Float Zone process. The upper part is the polysilicon rod and the lower part below the RF coil is the solidifying monocrystalline silicon rod

The Float Zone Process

Zone refining of crystals in order to increase the purity of the material has been known for more than half a century. The purification step takes advantage of the concentration change by segregation of most impurities during the liquid–solid transition. Many different purification techniques exist but one of the most fascinating is the freely floating zone refining method, where the floating zone is suspended between the melting polysilicon and the monocrystalline interfaces (Fig. 1). The Float Zone technology has been perfected for the growth of silicon monocrystalline material. Being freely floating with no contact to crucibles makes it possible to grow monocrystalline silicon with the highest purity which is important for a number of electronic and optoelectronic applications. Float Zone monocrystalline growth starts from a high purity, small diameter seed crystal. The seed is prepared in the right crystalline direction in order to grow pure silicon with a very small amount of crystalline defects.

Minimising Defects

The Float Zone process is run at significantly higher growth rates (v) than is the Czochralski process. Typically, the growth rate for Float Zone growth is 2-3 times higher than Czochralski growth rates. The v/G_s Voronkov number, where G_s is the axial temperature gradient at the monocrystal-melt interface, is thus very high and all Float Zone ingots are vacancy rich. The detailed vacancy size distribution and the detailed vacancy spatial distribution in the Float Zone silicon is highly dependent of the control of the solidifying molten silicon and especially on the cooling rate. The cooling rate ($v \times G_s$) determines how the individual vacancy clusters interact during cooling. Fast cooling can cause agglomerates of vacancies to form that disturb the perfect silicon lattice and can cause dislocations to form during subsequent device processing.

Slow cooling, on the other hand, stabilises the dynamics of the growth cycle and makes agglomeration less likely. If "dead zones" with little or no axial interchange between the surface of the melt and the solidifying molten silicon is present, these "dead zones" can also be attractive sites for increased defect concentration as well as acting as a drain for any contaminants present in the melt. Best scenario for defect control is therefore to assure maximum intermixing of the molten silicon before final solidification and to assure relatively slow cooling over as large a radial and axial distance of the Float Zone system as possible.

The crystalline defects in silicon can affect the properties of electronic devices. In polished wafers prepared from Czochralski silicon, the excess of interstitials and the high density of oxygen in the bulk are known to cause device failure unless special engineered silicon wafers are used. For polished wafers prepared from Float Zone silicon, the vacancy related defects can have an impact on the device yield in case of non-optimal growth recipes. For Preferred Float Zone silicon all parameters have been optimised so that

1) $v/G_s >> C_{crit}$ in all points and
2) $D(v/G_s) \approx 0$,

where C_{crit} is the critical value between predominantly interstitial defect types and predominantly vacancy defect types in the monocrystals. When both conditions 1) and 2) apply D-defects (or Flow Pattern Defects) are not present in the monocrystals and the thermally generated vacancy point defects are small in size but relatively high in density. The delineation of these small point defects has been done in platinum decoration experiments, where densities up to a few times 10^{13} cm^{-3} have been found.

Absence of D-defects (Flow Pattern Defects) is very important for device yield. D-defects from the growth process are known to cause failure in a Gate Oxide Integrity test. The GOI test consists of processing several identical MOS devices onto the polished wafer by oxidation and metallisation steps. Each individual MOS device is then tested for its maximum breakdown boundaries and the number of devices that survive relative to the total number of tested devices make up the GOI yield. In absence of D-defects, GOI yields in between 95-100% are expected. Results from a two part constant current test cycle (test 1: 60 $\mu A/cm^2$ for 70 ms and test 2: 1 mA/cm^2 for 500 ms) on a p-type PFZ wafer showed that the number of MOS capacitors that survived was 206 out of 209 processed (98.6%) and 203 out of 209 (97.1%) for test 1 and test 2, respectively. As expected for this optimised Float Zone growth process GOI yield is in excess of 95% that otherwise only can be achieved in specially engineered Czochralski wafers.

To support the GOI test results a defect selective Secco etching was made on a p-type PFZ wafer. In this case it was chosen to employ a prolonged Secco etching removing in excess of 20 µm of

silicon to be able to delineate a D-defect of any size. A normal Secco etch easily delineates the D-defects in Czochralski wafers, and the surface density of D-defects is measured by optical microscopy on predefined areas of the wafers. Fig. 2 shows results from measurement of D-defects on p-type PFZ wafers. No D-defects are observed in accordance with the results of the GOI yield testing.

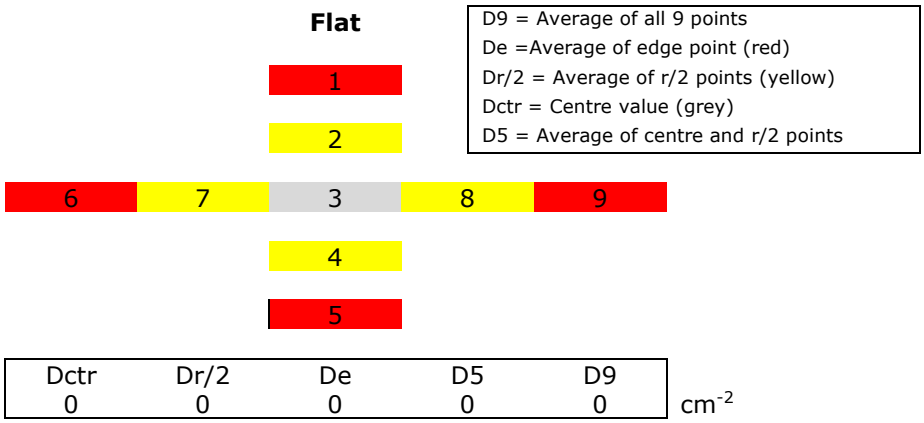


Figure 2. Delineation of D-defects (Flow Pattern Defect void density) by prolonged Secco etching.

Lifetime

The bulk minority carrier lifetime is a measure of the quality of the silicon crystal by measuring the recombination of light induced minority carriers with the bulk majority carriers (i.e. the background doping density).

Spatially resolved lifetime measurements can be used to verify that condition 2) above is a good approximation for the PFZ process. In case of large radial variances for the fundamental Voronkov number the radial variation of the bulk lifetime is expected to be high because the minority carrier lifetime is highly dependent on the vacancy distribution and density. In Fig. 3 is shown results for spatially resolved effective lifetime measurements on p-type PFZ crystal. The crystal is measured on the end faces of the crystal in discrete points. The results in Fig. 3 show that there is no radial variation of the bulk lifetime for PFZ products and thus the Voronkov number is close to constant in radius r. From Fig. 3 it is noted that the axial variation of the bulk lifetime is high and this is an indication of some variation of the Voronkov number with axial length z during the full growth cycle. However, as long as the effective bulk lifetime is in excess of 1000 µs for a p-type PFZ product the Voronkov number is sufficiently high to guarantee small vacancy point defects that have no impact on BMD or D-defect dynamics. D-defects are observed in accordance with the results of the GOI yield testing.

Very Low Oxygen Levels

Processing on Czochralski silicon wafers can have at least two negative effects on the properties of the electronic devices. First, a resistivity shift can occur that is associated with activation of thermal donors. Secondly, after finished device processing bulk micro defects (BMD) originating from impurity precipitation can cause device failures. Both of these effects are in part associated with oxygen in the bulk of the CZ silicon. To be able to deliver prime polished and epi-ready wafers that will not fail during device processing a thermal donor annihilation step together with an annealing step to suppress the formation of BMD's in the surface region must be performed. Using PFZ material these steps can be avoided. The oxygen content in Float Zone silicon in general is typically less than 10^{16} cm^{-3} just from the fact that the melt is not in contact with crucibles.

A test which is then relevant only for Czochralski wafers is the bulk defect analysis test which is used to delineate bulk micro defects (BMD's) associated with oxygen precipitates. The testing itself consists of a thermal cycling recipe in an inert/oxidising atmosphere and subsequent chemical etching (Schimmel) on cleaved wafers to measure the density of BMD's in the bulk silicon wafer and to measure the extent of the defect free zone close to the wafer surface (= denuded zone). In the denuded zone the BMD's have been suppressed by the thermal cycling process. As expected, testing on Float Zone wafers reveal no BMD's ($< 10^{6}$ cm^{-3} = detection limit) and therefore the extension of the BMD free zone is through the entire wafer.

Summarising on the findings of the Preferred Float Zone crystalline state, it is true that it is perfect by every means of measuring. The small sized vacancies have no impact on device properties as GOI yield is maximised, D-defects are absent from the bulk and BMD will not form in the bulk during thermal processing steps.

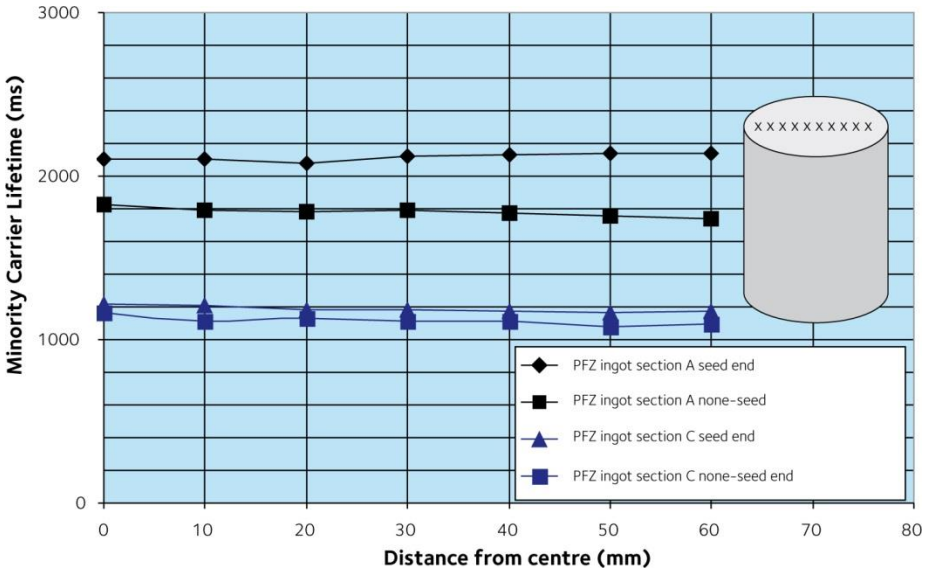


Figure 3. Radial variation of bulk minority carrier lifetime for (100) p-type PFZ material.

Precise Dopant Control

Perhaps the most important feature of the Float Zone technology in comparison with Czochralski technology is the ability to exactly control the resistivity throughout the whole of the crystal. This is in particular important for applications using the bulk of the silicon wafers in the making of electronic devices. There are two practical ways of obtaining the very good resistivity control for Float Zone crystals. One is by doping the crystals when they are pulled by introducing controllable amounts of gaseous dopants into the growth chamber. This technique is called in-situ doping or gas phase doping and is the basis for PFZ crystal growth.
The other technique is by doping the crystal after it has been pulled. This technique is called ex-situ doping and it is done in neutron irradiating reactors. The starting material for ex-situ doping is high resistivity silicon that after being irradiated with a controllable dose of neutrons changes its resistivity by transforming silicon atoms to phosphor dopant atoms. The ex-situ neutron transmutation doping (NTD) method is by far the most accurate in terms of resistivity control. Not only is the radial resistivity variation (RRV) extremely low, but also the ingot to ingot variation can be kept extremely low because of the ability to accurately control the neutron dose.

In-situ doping by gas inlets near the melt/crystalline interface is the best way to achieve reliable outcomes in volume production. By controlling the amount of high purity gas and by means of controlling the Float Zone process it is possible to achieve low resistivity variations almost at the same low levels as it is possible to achieve for NTD Float Zone products. This is especially the case for larger diameter growths where comparable resistivity tolerance levels of performance between PFZ and NTD products can be achieved. In this section it will be shown that PFZ processes have

excellent resistivity control over a large range of bulk resistivities. Unlike NTD products, PFZ products can be produced in n- and p-type versions using either group V or group III-based gas products for in-situ doping. Usually, phosphine is used for n-type in-situ doping and diboran is used for p-type insitu doping. The biggest difference in resistivity control is due to the fact that boron impurities are more readily segregated from the melt into the monocrystalline solid state phase than are the phosphorous impurities.

Fig. 4 shows a radial resistivity variation plot taken from a 150 mm PFZ n-type product. 9 wafers were cut from one end of ingot and they were each measured in 49 points across the wafer by 4 point probe measurements. There are several things to note from Fig 4. First, all points are lying in a narrow band with small or no systematic variation across the wafers. This is a very good indication of full control of the monocrystalline growth, since less controlled growth modes would result in large band variations. Secondly, for all of the 9 wafers measured the maximum radial resistivity variation (RRV) is below 7%. RRV is defined as

$$RRV = \frac{R_{MAX} - R_{MIN}}{R_{MIN}} \times 100\% \qquad (1)$$

Where R_{MAX} and R_{MIN} are the maximum and minimum resistivity within one wafer.

Fig. 4 clearly shows that the growth process is under control in that it can guarantee low RRV and no wafer-to-wafer systematic variance. The resistivity tolerance for the 9 wafers is very good, but is does not show the full variance along the ingot axis. The low effective segregation coefficient during growth (~0.3-0.5) will cause the phosphorous to accumulate in the melt thereby altering the concentration of phosphorous and hence the resistivity of the finished product. For n-type PFZ specifications it is possible to achieve a ±10% or lower total resistivity tolerance for 150 mm products.

Fig. 5 shows a radial resistivity variation plot taken from a 150 mm high resistivity p-type PFZ product. 2 wafers were cut from each ends of the ingot and they were each measured in 49 points across the wafer by 4 point probe measurements in a 0 and 90 degree direction. As was the case for the n-type PFZ product, all points are lying in a narrow band with small or no systematic variation across the wafers. Again, this is a very good indication of full control of the monocrystalline growth. As for the n-type PFZ product, the maximum radial resistivity variation (RRV) is below 7%.

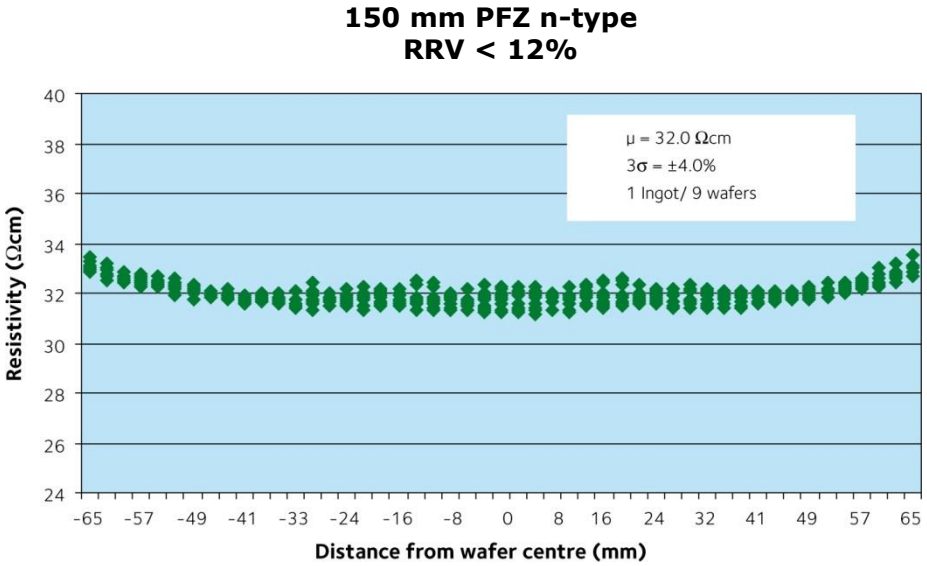


Figure 4. Radial resistivity variation plot for (100) n-type PFZ wafers

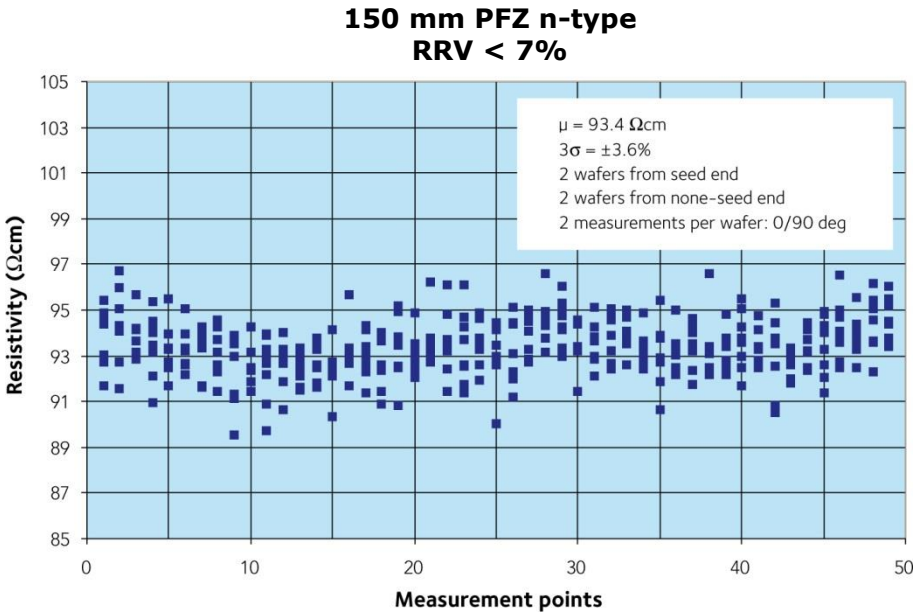


Figure 5. Resistivity tolerance plot for high resistivity (100) p-type PFZ wafers

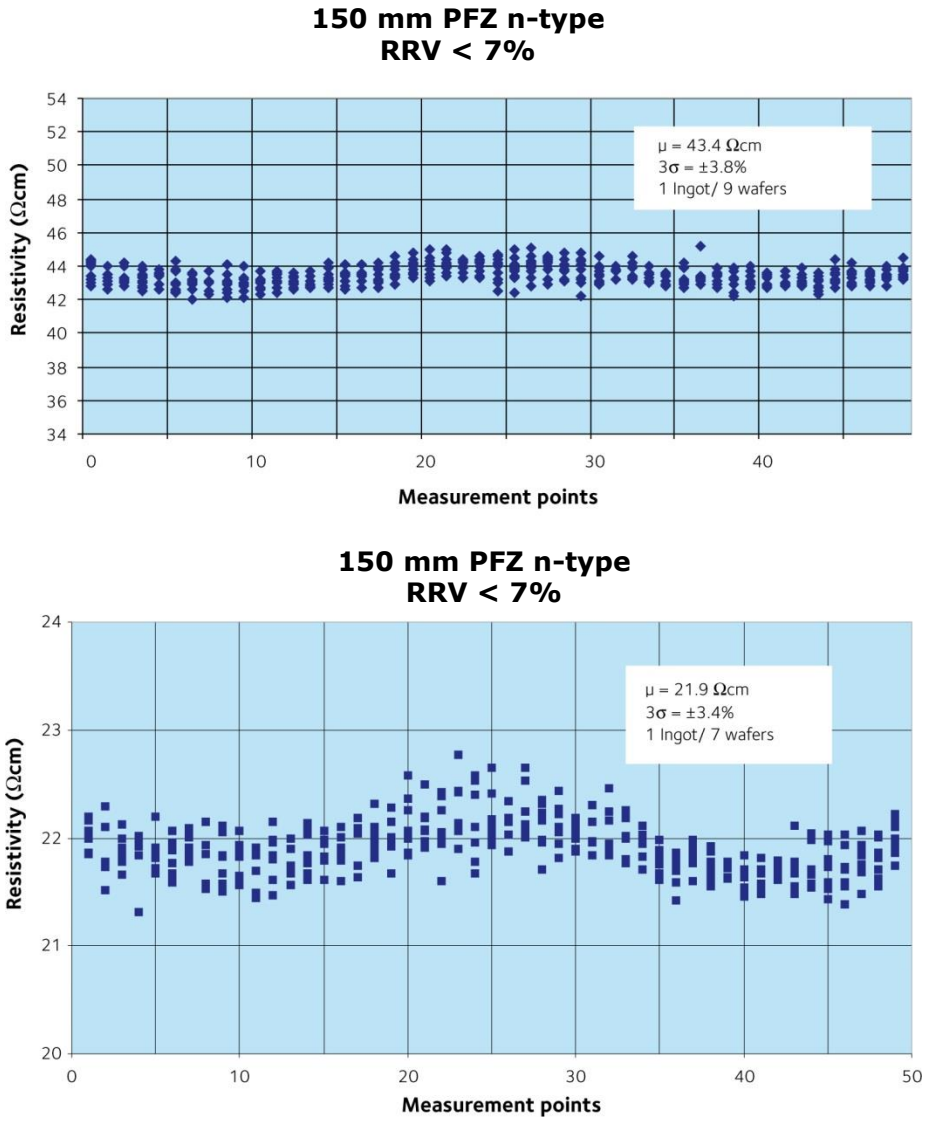


Figure 6. Radial resistivity variation plot for (100) p-type PFZ wafers

Fig. 6 shows similar resistivity plots for 150 mm p-type PFZ products as was shown in Fig. 5, but for lower target bulk resistivities. By comparison of the results shown in Figs. 5 and 6 it can be concluded that the p-type products have similar characteristics in a very broad resistivity range from 1-100 Ωcm. The upper limit is not restricted to 100 Ωcm, but is actually as high as 1000 Ωcm. In the broad resistivity range from 1-100 Ωcm it is possible to achieve resistivity tolerances of ±10% for 150 mm PFZ p-type products and in optimised cases a ±8% resistivity tolerance can be achieved.

N-type		Unit	Target resistivity range		
			1-100Ωcm	100-500Ωcm	500-1000Ωcm
Orientation			<111>*, <100>		
Resistivity tolerance	125 mm	%	±10	±13	±20
	150 mm		±8	±10	±20
	200 mm	%	±10	±15	±20
RRV	125 mm	%	<10 <100> <15 <111>	<18	<20
	150 mm		<9 ** (<12)***	<13 ** (<18)***	<20** (30)***
	200 mm	%	<14	<20	<25
Striations		%	±15	±20	±20
Minority carrier bulk lifetime		µs	>500	>1000	>1000

Table I. Resistivity capabilities for n-type PFZ products.

* <111> is not available in 150 mm diameter PFZ products
** Applies to 95% of all wafers
*** Applies to all wafers

N-type		Unit	Target resistivity range		
			1-100Ωcm	100-500Ωcm	500-1000Ωcm
Orientation			<111>*, <100>		
Resistivity tolerance	125 mm	%	±10	±13	±20
	150 mm		±8	±10	±20
	200 mm	%	±8	±10	±20
RRV	125 mm	%	<8 <100> <15 <111>	<18	<20
	150 mm		<8	<8	<10
	200 mm	%	<8	<10	<20
Striations		%	±10	±15	±15
Minority carrier bulk lifetime		µs	>200	>500	>500

Table II. Resistivity capabilities for p-type PFZ products.

*<111> is not available in 150 mm diamete

For both n-type and p-type PFZ products the resistivity limit is 1000 Ωcm, but can be extended to higher resistivity limits by proper combination of the PFZ growth process with Topsil HiRes® growth process. Table I and II summarises the full capability range for 125mm, 150mm, and 200mm n- and p-type PFZ products, respectively.

Summarising all of the findings above PFZ silicon makes perfect silicon wafers by all means of defining perfect silicon. Key features of PFZ wafers are

- Large bulk target resistivity range
- Low resistivity tolerances and record low radial resistivity variations
- High minority carrier lifetimes with low radial variation of the bulk lifetime
- Tolerant towards device processing
- Built-in control of defect levels – no D-defects and no BMD's

PFZ wafers can thus be used for many different applications in which the starting substrate heavily impacts on the finished device properties.

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Topsil Semiconductor Materials A/S

Topsil is a world leading supplier of ultrapure silicon to the global semiconductor industry. Engaging in long term relations with customers, Topsil focuses on premium quality, an efficient production process and a safe delivery of products.

Topsil targets mainly the power market on which it provides ultrapure silicon for the most demanding purposes, based on extensive knowledge and significant investments in new technology, facilities and equipment.

Headquartered in Copenhagen Cleantech Park, Topsil spans production sites in Denmark and Poland and sales locations in Europe, Asia and the US. Topsil is publicly listed at the Nasdaq OMX Copenhagen stock exchange and was founded in 1959.

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