EPITAXIAL WAFERS FOR HIGH PERFORMANCE DEVICES

Topsil Semiconductor Materials S.A. is a leading supplier of high quality Epitaxial wafers used in the semiconductor industry, specialized in the manufactures semiconductor-grade silicon ingots using Czochralski single crystal growth method and process substrates for advanced epitaxial wafers. The Epi wafers are used as substrates for low power, medium power and special devices. All Epi wafers are made according to customer specifications with custom made substrates and epitaxial layers in diameters of 150 mm, 125 mm, 100 mm, 76.2 mm

All wafers are customized and meet tight mechanical and electrical parameter specifications according to SEMI Standards. On customer request the wafers can be produced with tighter and different parameters.

PRODUCTION FACILITIES
Topsil Semiconductor Materials S.A. has a state-of-the art production facility to support all production steps from crystal growth to Epitaxial deposition and meets customer requirements for both large and small volumes.

Topsil Semiconductor Materials S.A. is a ISO 9001:2000 and ISO 14001:2004 certified company. The following are the scope of registrations of certificate numbers 04100 20021532/-E2 and 04104 20021532/-E2: “The production of electronic grade silicon single crystals and wafers for semiconductor industry.” Topsil has since 2002 been certified by TÜV CERT Certification Body of RWTÜV Systems GmbH.
Ingot growing

1. Charge preparation
The ultra high purity polysilicon is accurately weighed and prepared for melting in the furnace. Dopant is weighed and added to the silicon.

2. Crystal Growth
Crystal growing consists of four steps:
(a) setting up the furnace,
(b) placing the charge in the quartz crucible,
(c) closing and powering on the furnace,
(d) cool down and ingot removal. The final product of crystal growing is a structured ingot with nose and tail.

3. Ingot Heat Treatment
Heat treatment is done to anneal the ingot and to stabilize the resistivity readings. The ingot is heated at 650°C for one hour. This tends to stop the oxygen donor effect, which can affect the resistivity of the ingot and wafers. This process is conducted on 3 inch and most types of 4-inch ingots. For larger ingot diameters and certain types of 4-inch material the heat treatment is made on wafers after step # 22.

4. Ingot Cropping (Top and Tail)
The top and tail parts are cut from the ingot, making both ends of the ingot body perpendicular to the axis of growth.

5. Ingot Etching (Structure)
In this step, the ingot is given a light chemical etching and inspected for possible loss of structure.

6. Ingot Cropping (Structure)
If any portion of the ingot is not structured, it will be cropped off and discarded.

7. Ingot Oxygen and Carbon Content and Resistivity Measurement
The structured ingot is weighed. The resistivity is measured at both ends of the ingot and along the axis to determine if it is within specification. If necessary, measurements of oxygen and carbon content are carried out.

8. Ingot Cropping (Crop 2)
When the whole ingot does not meet specific resistivity or oxygen or carbon content requirements, the ingot is cut into various sections that meet specified parameters.

9. Ingot Cylindrical Grinding
The grinding operation removes all material in excess of the wafer required diameter.

10. Ingot X-ray
The ingot must be x-rayed to determine the exact crystal-line orientation. Once determined, a primary flat is ground.

11. Ingot Flatting
The major flat is ground along the length of the ingot to orient the wafers to a specified crystallographic axis. The secondary flat is made (if necessary).

12. Ingot Q.A. Inspection
After all ingot processing is completed, Q.A. inspection of the ingot is performed to ensure conformity to the appropriate specifications.

13. Ingot Etch
About 0.4 mm is removed during this process.
14. Ingot Mounting
The ingots are mounted on the beam before multi wire slicing.

15. Slicing
The ingots are moved downwards into the wire web. SiC slurry transported by tensioned steel wire (Ø140 microns) slices the ingots simultaneously into the wafers.

16. Wafer Slice Cleaning
After slicing, the wafers are cleaned to remove kerf, lubricants and other impurities.

17. Wafer Edge Rounding
An abrasive disc is used to eliminate the sharp edges left from slicing. This reduces wafer edge chipping and cracking. Standard (20°) and epi shape (11°) are used depending on customer specification.

18. Wafer Pre-Lap Thickness Sort
The wafers are sorted by thickness. The cleaned, “as cut” wafers are sorted incrementally into groups of 5 microns thickness. In addition, the material can be inspected for fractures and other cosmetic defects, which might jeopardize the lapping yield. TTV and WARP are also checked to eliminate defective wafers in the early stage of production.

19. Wafer Lapping
The sliced wafers are lapped to produce a flat surface (free of slicing damage) in preparation for etching and polishing. Both sides of the wafer are simultaneously lapped with an alumina slurry mixture.

20. Wafer Lap Cleaning
Lap cleaning is the same operation as slice washing. Lapping compounds and other contaminants are removed in a sequence of cleaning steps using solvents and de-ionized water and/or a light solution of KOH.

21. Wafer Etching
Any stress or structural damage, which may have occurred during slicing and lapping, is removed at this time. The wafers are chemically etched with either an acid (HF, HNO₃, CH₃COOH) or a base (KOH) solution to remove any residual damage and provide a clean surface.
Slicing, lapping and etching

22. Wafer Cleaning
Wafers are cleaned using DI water and low concentration chemicals.

O1. Wafer Heat Treatment (optional)
Certain types of wafers (compare point # 3) are heat-treated. After this operation the wafers return to operation #22.

O2. Hard Backside Damage – HBSD (optional)
Certain types of wafers (depending on customer specification) undergo the operation of hard backside damage. This operation is conducted by means of wet bead blasting. The material used is quartz. Hard backside damage operation creates the damaged layer for extrinsic gettering. After this operation the wafers return to operation #22.

23. Wafer Inspection
Wafers are inspected for cosmetic defects.

24. Wafer Sorting (Thickness and Resistivity)
The wafers are sorted for both thickness and resistivity. Rejected wafers are discarded. By sorting the wafers into groups of 5 microns increments, wafers of the same group can be scheduled for the correct amount of stock removal during wafer stock removal polishing.

25. Wafer Q.A. Inspection
The wafers are checked to ensure proper specifications before they are placed into the etched wafer production control inventory.

Wafer back side treatment staging

26. Wafer Back Side treatment Staging
(optional stage)
The backsides of the wafers can be sealed with Polysilicon layer and LTO layer.

O3. Wafer Poly and/or LTO layer (optional)
CVD polysilicon layer and/or Low Temperature Oxide can deposited on the wafers back. Alternatively one of the method can be chosen only, depending on customer demand. For customer request we prepare the oxide free exclusion ring in the wafers edge area.

O4. Layers inspection (optional)
Layer thickness and thickness variation can be checked using dedicated equipment.
Polishing, staging and polishing

27. Wafer Polishing Staging
   To eliminate lot mixing during the polishing process, wafers are separated according to lot number.

LM. Wafer Laser Marking (optional)
   Wafers are laser marked using “turn-key”, YAG laser marking system. Marking takes place on the front side of each wafer, typically along its primary flat. A variety of character types (fonts) are available, including SEMI OCR, which is ideally suited for use with various automatic readers.

28. Wafer Mounting
   The wafers are mounted and pressed onto polishing carriers.

29. Wafer Polishing
   Wafers are polished to a uniform thickness by removing their excess stock. Up to 20 microns is removed through this chemical/mechanical process. It is multistage operation, after the stock removal polishing, the wafers are polished to a mirror finish to eliminate haze defects.

30. Wafer De-mounting
   The wafers are then de-mounted from the carrier and placed into cassettes.

31. Wafer Cleaning
   After de-mounting, the wafers are processed through a cleaning operation including SC-1 and DI water sequence.

32. Wafer ADE Control
   Prior to the final cleaning, the wafers are subjected to a final noncontact check for resistivity, thickness, type, TIR, TTV, WARP, BOW etc. Automatic ADE WaferCheck system is used for this purpose.

33. Megasonic Cleaning
   The polished wafers are cleaned in a clean room environment. Megasonic cleaning process and quick dump technique assures particles and chemical residues removal from the wafers surfaces.

34. Inspection
   The wafers surfaces are visually inspected under high intensity light for defects such as scratches, chips, contamination/particulate, flakes, waviness, haze and orange peel. On request LPDs are checked with automatic Tencor 5500 scanning.
Epitaxy

35. Epitaxy Layer Deposition
The epitaxial layer is deposited on the wafers from a Trichlorosilane source gas or a Tetrachloride source gas, depending on customer demand. Dopant gases are Di-boran or Phosphin. The gas flows and process times are carefully chosen to achieve specified layer thickness, layer resistivity and required transition region profile.

36. Epitaxy Layer Inspection
The epi wafer surfaces are inspected under high intensity light for epi layer defects such as slips, haze, SF or nodules. 100% of wafers undergoing infrared epi thickness control in their centers and two or three wafers are measured in five points for statistical purposes. One wafer from the epi batch is checked for resistivity with mercury probe C-V control method. This wafer is separated from the lot, as the C-V control method is destructive. Alternatively the resistivity is measured with non-destructive QCS 7200RC system with wafer mapping capability.
Final wafer quality assurance

37. Final Wafer Quality Assurance
This is the final handling before customer inspection. Samples are taken on a statistical basis from the lots and inspected to verify the conformance of all electrical, geometrical and surface parameters according to customer and/or SEMI requirements.

Wafer packaging

38. Wafer Packaging
Immediately following the Final Wafer Quality Assurance, the wafers are enclosed in ultra pure containers and heat-sealed in polypropylene bags. The bags are put into packaging boxes and labeled with appropriate customer information. The boxes are closed.

Wafer shipping

39. Shipping to Customer
Only the best reliable forwarding agencies and airlines are chosen to secure quick, cheap and safe wafers transport to all customers. Wafers are shipped using any agreed terms according to Incoterms 2000.

Epitaxial wafers - substrates

| Orientation: | \(<111>, <100>\) |
| Geometrical parameters: | Customer specification or SEMI Standards |
| Thickness (typical): | 380 µm, 400 µm, 525 µm and 625 µm * |
| Typical Resistivity Range: | As-doped: 0.001 – 0.005 Ωcm* |
| | Sb-doped: 0.008 – 0.020 Ωcm* |
| | B-doped: 0.010 – 0.020 Ωcm* |
| | B-doped: 0.001 – 0.010 Ωcm* |
| Available Backside Finish: | Standard: acid or alkaline etched |
| | - Soft Back Side Damage (SBSD – short etch) |
| | - Hard Back Side Damage (HBSD – wet bead blasting) |
| | - Low Temperature Oxide sealed (LTO) |
| | - Thermal Oxide sealed |
| | - Advanced (HBSD + LTO) |
| | - Backside Multilayers (PolySi + LTO) |
| | - Option for LTO and Advanced – Oxide free exclusion ring |
| | - EPI polysilicon layer deposited in situ in the reactor (2÷20 µm) |

* - Other specs available on customer’s request
# Epitaxial wafers - substrate details

<table>
<thead>
<tr>
<th>Property</th>
<th>unit</th>
<th>3&quot;</th>
<th>4&quot;</th>
<th>5&quot;</th>
<th>6&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Both Sides</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diameter tolerance Std</td>
<td>mm</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.2</td>
<td>±0.2</td>
</tr>
<tr>
<td>Diameter tolerance Min</td>
<td>mm</td>
<td>±0.2</td>
<td>±0.2</td>
<td>±0.2</td>
<td>±0.1</td>
</tr>
<tr>
<td><strong>Frontside</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimal thickness</td>
<td>µm</td>
<td>300</td>
<td>290</td>
<td>400</td>
<td>400</td>
</tr>
<tr>
<td>Maximal thickness</td>
<td>µm</td>
<td>1200</td>
<td>1200</td>
<td>1200</td>
<td>1200</td>
</tr>
<tr>
<td>Tolerance Std</td>
<td>µm</td>
<td>±25</td>
<td>±25</td>
<td>±25</td>
<td>±25</td>
</tr>
<tr>
<td>Tolerance Min</td>
<td>µm</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>Typical TTV</td>
<td>µm</td>
<td>&lt; 5</td>
<td>&lt; 5</td>
<td>&lt; 5</td>
<td>&lt; 5</td>
</tr>
<tr>
<td>Maximum TTV</td>
<td>µm</td>
<td>&lt; 10</td>
<td>&lt; 8</td>
<td>&lt; 8</td>
<td>&lt; 8</td>
</tr>
<tr>
<td>Typical TIR</td>
<td>µm</td>
<td>&lt; 5</td>
<td>&lt; 4</td>
<td>&lt; 4</td>
<td>&lt; 4</td>
</tr>
<tr>
<td>Maximum TIR</td>
<td>µm</td>
<td>&lt; 10</td>
<td>&lt; 6</td>
<td>&lt; 6</td>
<td>&lt; 6</td>
</tr>
<tr>
<td>STIR*</td>
<td>µm</td>
<td>&lt; 1</td>
<td>&lt; 1</td>
<td>&lt; 1</td>
<td>-</td>
</tr>
<tr>
<td>Bow</td>
<td>µm</td>
<td>&lt; 40</td>
<td>&lt; 40</td>
<td>&lt; 40</td>
<td>&lt; 40</td>
</tr>
<tr>
<td>Warp</td>
<td>µm</td>
<td>&lt; 40</td>
<td>&lt; 40</td>
<td>&lt; 40</td>
<td>&lt; 40</td>
</tr>
<tr>
<td><strong>Backside</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTO APCVD</td>
<td>Å</td>
<td>4000-9000</td>
<td>4000-9000</td>
<td>4000-9000</td>
<td>-</td>
</tr>
<tr>
<td>LTO Tolerance</td>
<td>%</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
<td>-</td>
</tr>
<tr>
<td>Edge exclusion</td>
<td>mm</td>
<td>0.3-2</td>
<td>0.3-2</td>
<td>0.3-2</td>
<td>-</td>
</tr>
<tr>
<td>Poly Si Std LPCVD</td>
<td>µm</td>
<td>0.8-1.2</td>
<td>0.8-1.2</td>
<td>0.8-1.2</td>
<td>-</td>
</tr>
<tr>
<td>Poly Si Tolerance</td>
<td>µm</td>
<td>±0.2</td>
<td>±0.2</td>
<td>±0.2</td>
<td>-</td>
</tr>
<tr>
<td><strong>Both Sides</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Oxide</td>
<td>Å</td>
<td>500-22000</td>
<td>500-22000</td>
<td>500-22000</td>
<td>500-22000</td>
</tr>
<tr>
<td>Oxide Tolerance</td>
<td>%</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
</tr>
</tbody>
</table>

* STIR @ 15x15 mm "Site best fit"

LPD automated scanning Max 10 @ > 0.3+1.0 µm (capability for 4", 5" and 6")
## Epitaxial wafers - substrate details

<table>
<thead>
<tr>
<th>Property</th>
<th>unit</th>
<th>3”</th>
<th>4”</th>
<th>5”</th>
<th>6”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter tolerance Std</td>
<td>mm</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.2</td>
<td>±0.2</td>
</tr>
<tr>
<td>Diameter tolerance Min</td>
<td>mm</td>
<td>±0.2</td>
<td>±0.2</td>
<td>±0.2</td>
<td>±0.1</td>
</tr>
<tr>
<td><strong>Frontside</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimal thickness</td>
<td>µm</td>
<td>300</td>
<td>290</td>
<td>400</td>
<td>400</td>
</tr>
<tr>
<td>Maximal thickness</td>
<td>µm</td>
<td>1200</td>
<td>1200</td>
<td>1200</td>
<td>1200</td>
</tr>
<tr>
<td>Tolerance Std</td>
<td>µm</td>
<td>±25</td>
<td>±25</td>
<td>±25</td>
<td>±25</td>
</tr>
<tr>
<td>Tolerance Min</td>
<td>µm</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>Maximum TTV**</td>
<td>µm</td>
<td>&lt;10</td>
<td>&lt;10</td>
<td>&lt;8</td>
<td>&lt;8</td>
</tr>
<tr>
<td>Maximum TIR**</td>
<td>µm</td>
<td>&lt;10</td>
<td>&lt;8</td>
<td>&lt;6</td>
<td>&lt;6</td>
</tr>
<tr>
<td>STIR*</td>
<td>µm</td>
<td>&lt;1</td>
<td>&lt;1.5</td>
<td>&lt;1.5</td>
<td></td>
</tr>
<tr>
<td>Bow**</td>
<td>µm</td>
<td>&lt;40</td>
<td>&lt;40</td>
<td>&lt;40</td>
<td>&lt;60</td>
</tr>
<tr>
<td>Warp**</td>
<td>µm</td>
<td>&lt;40</td>
<td>&lt;40</td>
<td>&lt;40</td>
<td>&lt;60</td>
</tr>
<tr>
<td><strong>Backside</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTO APCVD</td>
<td>Å</td>
<td>4000-9000</td>
<td>4000-9000</td>
<td>4000-9000</td>
<td></td>
</tr>
<tr>
<td>Tolerance</td>
<td>%</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
<td></td>
</tr>
<tr>
<td>Edge exclusion</td>
<td>mm</td>
<td>0.3-2</td>
<td>0.3-2</td>
<td>0.3-2</td>
<td></td>
</tr>
<tr>
<td>Poly Si Std LPCVD</td>
<td>µm</td>
<td>0.8-1.2</td>
<td>0.8-1.2</td>
<td>0.8-1.2</td>
<td></td>
</tr>
<tr>
<td>Tolerance</td>
<td>µm</td>
<td>±0.2</td>
<td>±0.2</td>
<td>±0.2</td>
<td></td>
</tr>
<tr>
<td><strong>Both Sides</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Oxide</td>
<td>Å</td>
<td>500-22000</td>
<td>500-22000</td>
<td>500-22000</td>
<td>500-22000</td>
</tr>
<tr>
<td>Tolerance</td>
<td>%</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
</tr>
</tbody>
</table>

* STIR @ 15x15 mm “Site best fit”

** For wafers, which have resistivity greater than 3 kΩ*cm we can measure thickness in central point only, and we cannot measure **parameters.

LPD automated scanning Max 10 @ > 0.3÷1.0 µm (capability for 4”, 5” and 6”)

Laser Marking according to SEMI Standard or customer requirements
Final wafers - layers

EPI REACTORS: Epi Pro 5000 the latest generation of pancake reactors made by CSD (former Mattson) and Gemini 2 units

SILICON SOURCES: SiCl₄, SiHCl₃

DOPANT GASES: PH₃, B₂H₆

DEPOSITION RATE CONTROL: achieved by the source gas temperature and flow control (Typically 1 µm/min for SiCl₄ and 1.5 µm/min for SiHCl₃)

DIAMETER RANGE: 150 mm, 125 mm, 100 mm and 76.2 mm

STANDARD EPI LAYER PARAMETERS:

<table>
<thead>
<tr>
<th>Type</th>
<th>Thickness</th>
<th>Resistivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>n type epi layer</td>
<td>up to 150 µm</td>
<td>0.15÷100 Ωcm</td>
</tr>
<tr>
<td>Sb doped - substrates</td>
<td>up to 150 µm</td>
<td>0.2÷100 Ωcm</td>
</tr>
<tr>
<td>As doped substrates</td>
<td>up to 150 µm</td>
<td>0.10÷150 Ωcm</td>
</tr>
<tr>
<td>p type epi layer</td>
<td>up to 150 µm</td>
<td>up to 400 Ωcm</td>
</tr>
<tr>
<td>B doped substrates</td>
<td>up to 150 µm</td>
<td></td>
</tr>
<tr>
<td>Special epi layers and multi-layers</td>
<td>up to 150 µm</td>
<td></td>
</tr>
</tbody>
</table>

Epitaxial wafers – details

The epitaxial wafer specifications are divided into parameters concerning:

- substrate dopant
- back surface sealing
Table 1: MT Poly Sealed Epitaxial wafers specification

<table>
<thead>
<tr>
<th>Substrate</th>
<th>dopant</th>
<th>Back side seal</th>
<th>EPI wafer structure</th>
<th>Thickness min</th>
<th>Thickness max</th>
<th>EPI min</th>
<th>EPI max</th>
<th>Resitivity min</th>
<th>Resitivity max</th>
<th>RRV min</th>
<th>RRV max</th>
<th>RTV min</th>
<th>RTV max</th>
<th>Thickness tolerance</th>
<th>Thickness tolerance</th>
<th>RTV tolerance</th>
<th>RRV tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>As</td>
<td>MT poly</td>
<td>N/N+</td>
<td>0.2 **</td>
<td>70</td>
<td>70</td>
<td>3</td>
<td>150</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>+6±5 for T range 3 ÷ 50</td>
<td>±6±5 for T range 3 ÷ 50</td>
<td>7±6 for T range 3 ÷ 50</td>
<td>7±6 for T range 3 ÷ 50</td>
<td>±8±6 Ωcm</td>
<td>±8±6 Ωcm</td>
<td>±15 for R range 15.1 ÷ 70</td>
<td>±15 for R range 15.1 ÷ 70</td>
</tr>
<tr>
<td>Sb</td>
<td>MT Poly</td>
<td>N/N+</td>
<td>0.15</td>
<td>800</td>
<td>800</td>
<td>3</td>
<td>150</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>+6±5 for T range 3 ÷ 50</td>
<td>±6±5 for T range 3 ÷ 50</td>
<td>5±6±5 for T range 3 ÷ 50</td>
<td>5±6±5 for T range 3 ÷ 50</td>
<td>±8±6 Ωcm</td>
<td>±8±6 Ωcm</td>
<td>±15 for R range 15.1 ÷ 100</td>
<td>±15 for R range 15.1 ÷ 100</td>
</tr>
<tr>
<td>B</td>
<td>MT Poly</td>
<td>N/P-</td>
<td>0.5</td>
<td>800</td>
<td>800</td>
<td>5</td>
<td>150</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>+6±5 for T range 3 ÷ 50</td>
<td>±6±5 for T range 3 ÷ 50</td>
<td>7±6±5 for T range 3 ÷ 50</td>
<td>7±6±5 for T range 3 ÷ 50</td>
<td>±8±6 Ωcm</td>
<td>±8±6 Ωcm</td>
<td>±15 for R range 15.1 ÷ 100</td>
<td>±15 for R range 15.1 ÷ 100</td>
</tr>
<tr>
<td>B</td>
<td>MT Poly</td>
<td>N/P+</td>
<td>0.1</td>
<td>200</td>
<td>200</td>
<td>5</td>
<td>150</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>±5 for R range 0.5 ÷ 5</td>
<td>+6±5 for T range 3 ÷ 50</td>
<td>±6±5 for T range 3 ÷ 50</td>
<td>7±6±5 for T range 3 ÷ 50</td>
<td>7±6±5 for T range 3 ÷ 50</td>
<td>±8±6 Ωcm</td>
<td>±8±6 Ωcm</td>
<td>±15 for R range 15.1 ÷ 200</td>
<td>±15 for R range 15.1 ÷ 200</td>
</tr>
</tbody>
</table>

Notes:
* 0.05 Ωcm for monthly orders > 1000 pcs.
** 0.015 Ωcm for monthly orders > 1000 pcs.

Standard RRV and RTV is calculated from center point value and 4 points values, located 10 mm or less from the edge (see Drawing 1).

The formula is: (max-min)/(max+min)*100%
### Table 2: LTO Sealed Epitaxial wafers specification

<table>
<thead>
<tr>
<th>Substrate dopant</th>
<th>Back side seal</th>
<th>EPI wafer structure</th>
<th>R EPI min</th>
<th>R EPI max</th>
<th>Thickness EPI min</th>
<th>Thickness EPI max</th>
<th>Resistivity tolerance</th>
<th>RRV max</th>
<th>Thickness tolerance</th>
<th>RTV max</th>
<th>Substrate resistivity range</th>
</tr>
</thead>
<tbody>
<tr>
<td>As</td>
<td>LTO</td>
<td>N/N+</td>
<td>0.2 *</td>
<td></td>
<td>35</td>
<td>3</td>
<td>85</td>
<td>±5 for R range 0.2 ÷ 1</td>
<td>5</td>
<td>±6 for T range 3 ÷ 50</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±8 for R range 1.1 ÷ 10</td>
<td>8</td>
<td>±8 for T range 50.1 ÷ 85</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±15 for R range 10.1 ÷ 35</td>
<td>15 **</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sb</td>
<td>LTO</td>
<td>N/N+</td>
<td>0.2</td>
<td></td>
<td>100</td>
<td>3</td>
<td>100</td>
<td>±5 for R range 0.2 ÷ 15</td>
<td>7</td>
<td>±6 for T range 3 ÷ 50</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±8 for R range 15.1 ÷ 100</td>
<td>15 **</td>
<td>±10 for T range 50.1 ÷ 100</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±15 for R range 10 ÷ 35</td>
<td>15 **</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>LTO</td>
<td>N/P-</td>
<td>0.5</td>
<td></td>
<td>100</td>
<td>5</td>
<td>100</td>
<td>±5 for R range 0.5 ÷ 15</td>
<td>7</td>
<td>±6 for T range 3 ÷ 50</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±8 for T range 15.1 ÷ 100</td>
<td>15 **</td>
<td>±10 for T range 50.1 ÷ 100</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±15 for R range 15 ÷ 35</td>
<td>15 **</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>LTO</td>
<td>N/P+</td>
<td>1</td>
<td></td>
<td>35</td>
<td>5</td>
<td>100</td>
<td>±5 for R range 1 ÷ 5</td>
<td>12.5</td>
<td>±6 for T range 3 ÷ 50</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±8 for T range 5.1 ÷ 15</td>
<td>12.5</td>
<td>±10 for T range 50.1 ÷ 100</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±15 for R range 15.1 ÷ 35</td>
<td>15 **</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>LTO</td>
<td>P/P+</td>
<td>0.1</td>
<td></td>
<td>50</td>
<td>5</td>
<td>100</td>
<td>±5 for R range 0.1 ÷ 15</td>
<td>7</td>
<td>±6 for T range 3 ÷ 50</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±8 for T range 15.1 ÷ 50</td>
<td>15 **</td>
<td>±10 for T range 50.1 ÷ 100</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±15 for R range 15.1 ÷ 35</td>
<td>15 **</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>LTO</td>
<td>P/P+</td>
<td>0.1 **</td>
<td></td>
<td>35</td>
<td>5</td>
<td>85</td>
<td>±5 for R range 0.1 ÷ 5</td>
<td>7</td>
<td>±6 for T range 3 ÷ 50</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±8 for T range 5.1 ÷ 15</td>
<td>7</td>
<td>±10 for T range 50.1 ÷ 85</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±15 for R range 15.1 ÷ 35</td>
<td>15 **</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:  
* 0.05 Ωcm for monthly orders > 1000 pcs  
** 0.015 Ωcm for monthly orders > 1000 pcs  
*** RRV measurement pattern: center and R/2  
Standard RRV and RTV is calculated from center point value and 4 points values, located 10 mm or less from the edge (see Drawing 1).  
The formula is: (max-min)/(max+min)*100%
Epitaxial wafers – quality control

In the Epi Wafer production the epitaxial layer deposition process is a very important step. Perfectness of the layer depends strongly on ingot and substrate quality. Cemat has the control of the complete technology from crystal pulling of dedicated INGOTS, following the process of making prime, epi ready SUBSTRATES and the deposition of the EPI LAYERS. The technology is based on more than 20 years of experience, state of art equipment and quality control systems meeting the industry standards. This enable Cemat to produce high performance customized EPITAXIAL SILICON WAFERS. All designed according to the customer specification.

The quality control of ready EPI products follows SEMI Standards and ASTM standards requirements. Full lot control is guaranteed and historical data are kept. Statistical data are available upon request.

Production of Epi wafers is controlled in two levels: a standard process control (level 1) and a detailed control (level 2).

For level 1 control plan, the Epi layer thickness is measured on 2 or 3 wafers in 5 points and the rest of wafers in one point (measurement in the centre of the wafer) and the resistivity is controlled on 1 wafer from the run, the measurement is also performed in 5 points pattern. From these results the average Epi layer thickness and RTV, the average R and RRV are calculated. The statistical control of the process is based on this data. The Cp and Cpk are calculated.

For level 2 process control, wafer thickness is measured in 5 points and 1 wafer (or 2 wafers or 3 wafers) is measured for resistivity in 5 points. 5-point measurements consist of 1 measurement in the centre and 4 measurements in the distance of 5-10 mm from the wafer edge (or in half radius). These data are then processed to establish wafer-to-wafer and within-wafer uniformity of resistivity and thickness. The Cp and Cpk are calculated.

In case of small quantity order, new products and new customers or critical products only level 2 control plan is applied.
Epitaxial wafers – quality control equipment

Thickness measurements – FTIR (5 mm edge exclusion)
tools: QS 408 M (Biorad)
      QS 500 (Biorad)

Resistivity measurements:

C-V mercury probe (5 mm edge exclusion), 4-point probe on test wafers
acceptable in case of Within Wafer Uniformity determination
tool: SPCV-2000

EPI monitoring tool measures wafer resistivity using an advanced surface photo-voltage
technology. Non-destructive and non-contact measurement technique
tool: QCS 7200RC

Profile Determination Spreading Resistance (SRP)
tool: SPR-2000

Structure Evaluation acc. to ASTM F 1049-90 – Level A. This method covers the evaluation of epi wafer
quality in terms of haze and structural defects after heat treatment (oxidation)

Definitions for uniformity evaluation

Measurement pattern:
5 points cross, perpendicular to wafer flat, 1 point located in the centre and 4 points 5 mm in from wafer edge,
flat to be loaded to outside of susceptor pocket

Within Wafer Uniformity
5 points ((max-min)/(max+min)) x 100

Wafer to Wafer Uniformity
Using average value, 5 points, for each wafer in full run

Run to Run Uniformity
Using average value for all wafers in a run, for 3 sequential runs

Drawing 1: Location of 5 EPI measurement points
Epitaxial wafers - sample SRP’s
TOPSIL SEMICONDUCTOR MATERIALS S.A - PART OF TOPSIL GROUP

Topsil Semiconductor Materials S.A. is part of Topsil Group (Topsil) which is a world leading supplier of ultrapure silicon to the global semiconductor industry. Engaging in long term relations with customers, Topsil focuses on premium quality, an efficient production process and a safe delivery of products. Topsil primarily manufactures float zone and czochralski silicon wafers for the Power Market – from Mega Watt to milli Watt. In addition, Topsil supplies a number of specialty products dedicated for MEMS, detector, communication and Photo Voltaic markets.

Topsil is headquartered in Copenhagen Cleantech Park, Denmark, with production sites in Denmark and Poland and sales location in Europe, Asia and the US. Topsil is a public listed company at Nasdaq OMX Copenhagen stock exchange.

Milestones
1958: First production of Float Zone silicon (Topsil)
1964: Czochralski growing of Si and Ge (Formerly Cemat, now: Topsil Semiconductor Materials S.A.)
1970: Foundation of CeMat’70 - materials for electronics including silicon (Topsil S.A.)
1973: NTD range, first to market (Topsil)
1988: 150 mm Float Zone crystal (Topsil)
1992: Foundation of Cemat Silicon SA as a private Joint-Stock-Company (Topsil S.A.)
1993: Introduction of 3” and 4” Prime wafers (Topsil S.A.)
1994: 4” EPI products (Topsil S.A.)
1997: Computer controlled Float Zone process introduced (Topsil)
1998: P-FZ ±10% introduced (Topsil)
       6” Prime wafer range (Topsil S.A.)
2001: Design and construction of new generation of FZ puller with 200 mm capacity (Topsil)
2002: PV-FZ for the photovoltaic market (Topsil)
2003: HiRes™ for RF MEMS applications (Topsil)
2004: 6” EPI range (Topsil S.A.)
2007: Start of 6” EPI volume production (Topsil)
2008: Topsil acquires Topsil S.A.
2010: Expansion of FZ production facilities (Topsil)
2012: Formal name change to Topsil Semiconductor Materials S.A. (Topsil S.A.)

Competencies
50+ year’s experience in the semiconductor industry
Continuous R&D of products and processes to meet the increasing customer demand
Experienced in joint development with Customers
Flexible production facilities
Leading edge proprietary Float Zone and Epi technology

Products
NTD    Neutron Transmutation Doped silicon for very high power devices
PFZ    Preferred Float Zone for Power applications
HPS    High Resistivity Silicon for Detector applications
HiRes* High Resistivity silicon for communication devices
HiTran* High Transparency silicon for Infra Red applications
PV-FZ* Photo Voltaic Float Zone for high efficiency solar cells
CZ Epi Medium and low power devices
CZ Mem High precision substrates for MEMS devices.

TOPSIL SEMICONDUCTOR MATERIALS S.A - PART OF TOPSIL GROUP

Competencies
50+ year’s experience in the semiconductor industry
Continuous R&D of products and processes to meet the increasing customer demand
Experienced in joint development with Customers
Flexible production facilities
Leading edge proprietary Float Zone and Epi technology

Products
NTD    Neutron Transmutation Doped silicon for very high power devices
PFZ    Preferred Float Zone for Power applications
HPS    High Resistivity Silicon for Detector applications
HiRes* High Resistivity silicon for communication devices
HiTran* High Transparency silicon for Infra Red applications
PV-FZ* Photo Voltaic Float Zone for high efficiency solar cells
CZ Epi Medium and low power devices
CZ Mem High precision substrates for MEMS devices.

TOPSIL SEMICONDUCTOR MATERIALS S.A - PART OF TOPSIL GROUP

Competencies
50+ year’s experience in the semiconductor industry
Continuous R&D of products and processes to meet the increasing customer demand
Experienced in joint development with Customers
Flexible production facilities
Leading edge proprietary Float Zone and Epi technology

Products
NTD    Neutron Transmutation Doped silicon for very high power devices
PFZ    Preferred Float Zone for Power applications
HPS    High Resistivity Silicon for Detector applications
HiRes* High Resistivity silicon for communication devices
HiTran* High Transparency silicon for Infra Red applications
PV-FZ* Photo Voltaic Float Zone for high efficiency solar cells
CZ Epi Medium and low power devices
CZ Mem High precision substrates for MEMS devices.